ST6G3238E

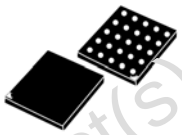
Dual supply level translator for SD / MiniSD / T-Flash with ±8 kV contact discharge ESD protection

Features

- High speed: t_{PD} = 4.4 ns (typ.) at T_A = 85 °C
  V_{CCB} = 2.7 V; V_{CCA} = 1.8 V
- Low power dissipation:
  $I_{CCA} = I_{CCB}$ = 5 µA (max.) at T_A = 85 °C
- Balanced propagation delays: $T_{PLH} \approx T_{PHL}$
- Power-down protection on inputs and outputs
- 26 Ω series resistor on A side
- EMI filter on B side
- Integrated pull-up and pull-down resistor on B side
- Operating voltage range:
  - V_{CCA} (opr) = 1.4 V to V_{CCB}
  - V_{CCB} (opr) = 1.4 V to 3.6 V
- Latch-up performance exceeds 500 mA (JESD17)
- ESD protection for card side (B port, CD and WP pins) ±8 kV, IEC 61000-4-2 ESD or contact discharge:
  HBM > ±15 kV (MIL STD 883 method 3015)
- ESD protection on A-port:
  HBM > ±2 kV (MIL STD 883 method 3015)
- RoHS compliant for µTFBGA25 package



TSSOP24



µTFBGA25

Description

The ST6G3238E is a dual supply low voltage CMOS level translator for SD / MiniSD / T-Flash fabricated with sub-micron silicon gate and five-layer metal wiring C^2MOS technology. Designed for use as an interface between a 3.3 V bus and a 2.5 V or 1.8 V bus in a mixed 3.3 V/1.8 V, 3.3 V/2.5 V and 2.5 V/1.8 V supply systems, it achieves high speed operation while maintaining the CMOS low power dissipation. The A port is designed to track V_{CCA}. The B port is designed to track V_{CCB}.

This device is intended for two-way asynchronous communication between data buses and the direction of data transmission is determined by CMD-dir / DATA0-dir / DAT123-dir inputs. The B port interfaces with the 3 V bus, while the A port interfaces with the 2.5 V and 1.8 V bus.

All inputs are equipped with circuits to protect against static discharge, giving them ±2 kV (on A-side except CD and WP pins) and ±15 kV (on B side, CD and WP pins) ESD immunity and transient excess voltage. See the section on integrated ESD protection and resistors for more information.

Obsolete Product(s) - Obsolete Product(s)

Table 1. Device summary

Order code	Package	Packaging
ST6G3238ETTR	TSSOP24	Tape and reel
ST6G3238ETBR	µTFBGA25	Tape and reel

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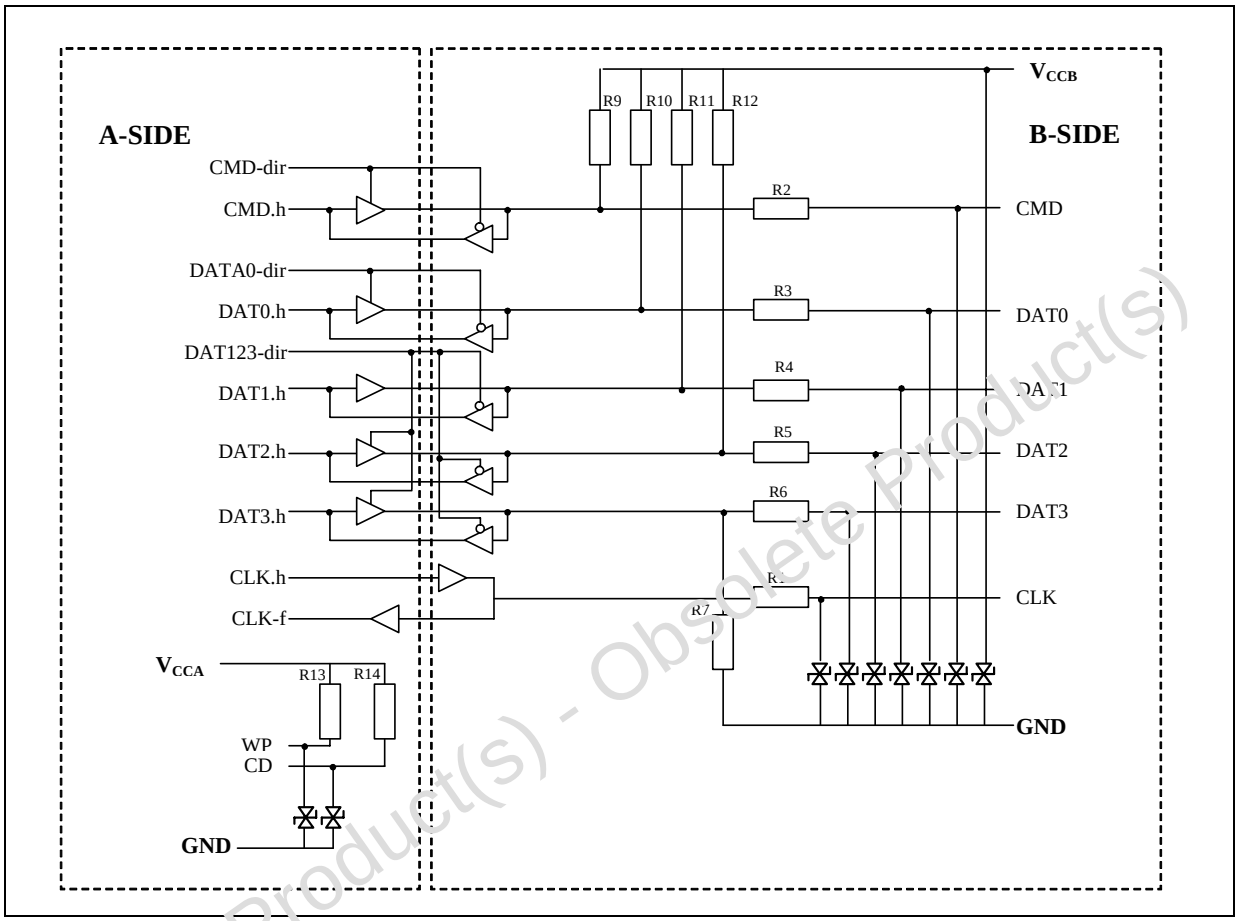
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Obsolete Product(s) - Obsolete Product(s)

1 Logic diagram

Figure 1. Block diagram



Obsolete Product(s) - Obsolete Product(s)

Table 2. Integrated ESD protection and resistor on B side

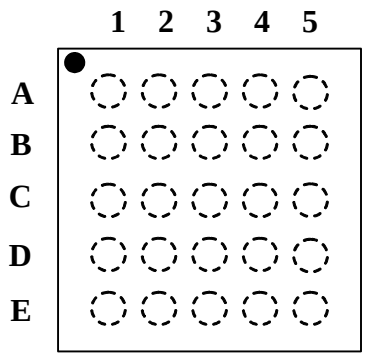
Resistors	Value	Bi-directional Zener diodes	
R1, R2, R3, R4, R5, R6	40 Ω	Vbr min.	14 V @ 1 mA
Tolerance	±20%	Line capacitance	< 20 pF
R10, R11, R12	70 kΩ		
R9	15 kΩ		
R7	470 kΩ		
Tolerance	±30%		

Table 3. Integrated pull-up resistors on WP and CD pins on A side

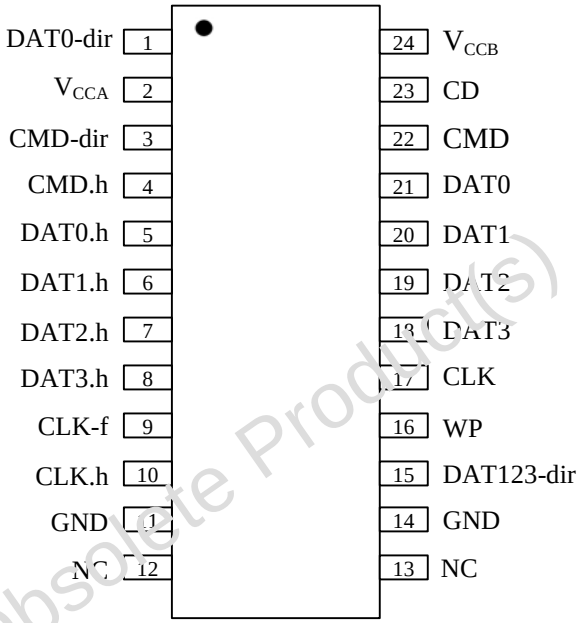
Resistors	Value
R13	100 kΩ
R14	100 kΩ
Tolerance	±30%

2 Pin connection and function

Figure 2. Pin connection (top through view for µTFBGA25 and TSSOP24)



µTFBGA25



TSSOP24

	1	2	3	4	5
A	DAT2.h	CMD-dir	DAT0.dir	NC	DAT2
B	DAT3.h	NC	V_{CCA}	V_{CCB}	DAT3
C	CLK.h	NC	GND	GND	CLK
D	DAT0.h	CMD.h	CD	CMD	DAT0
E	DAT1.h	CLK-f	DAT123-dir	WP	DAT1

µTFBGA25

Obsolete Product(s) - Obsolete Product(s)

2.1 Pin function

- CMD: Command is a bi-directional line. The host and card drivers operate in push-pull mode.
- DAT0-3: Data lines are bi-directional lines. The host and the card drivers operate in push-pull mode.

- CLK: Clock is a host-to-card signal. CLK operates in push-pull mode.
- Feedback (return) Clock is a feedback clock signal from the level shifter to host for controlling delays.
- CD: Card detect pulls HIGH state of input to V_{CCA}. This pin is protected against ESD up to 8 kV contact.
- WP: Write protect pulls HIGH state of input to V_{CCA}. This pin is protected against ESD up to 8 kV contact.

Table 4. Pin description

µTFBGA pin n°	TSSOP pin n°	Type	Side	Symbol	Name and function
A2	3	I	A side	CMD-dir	Command direction HIGH = A to B LOW = B to A
D2	4	I/O	A side	CMD.h	A-side command
D4	22	I/O	B side	CMD	B-side command
A3	1	I	A side	DAT0-dir	Data direction HIGH = A to B (write) LOW = B to A (read)
D1	5	I/O	A side	DAT0.h	Data input / output
D5	21	I/O	B side	DAT0	Data input / output
E3	15	I	A side	DAT123-dir	Data direction HIGH = A to B (write) LOW = B to A (read)
E1	6	I/O	A side	DAT1.h	Data input / output
A1	7	I/O	A side	DAT2.h	Data input / output
B1	8	I/O	A side	DAT3.h	Data input / output
E5	20	I/O	B side	DAT1	Data input / output
A5	19	I/O	B side	DAT2	Data input / output
B5	18	I/O	B side	DAT3	Data input / output
C1	10	I	A side	CLK.h	Clock input
C5	17	O	B side	CLK	Clock output
E2	9	O	A side	CLK-f	Clock feedback
D3	23	-	A side	CD	Card detect
E4	16	-	A side	WP	Write protect
B3	2	-	A side	V_{CCA}	Power supply
B4	24	-	B side	V_{CCB}	Power supply
C3, C4	11, 14	-	-	GND	Ground (0 V)
A4, B2, C2	12, 13	-	-	NC	No connect

Obsolete Product(s) - Obsolete Product(s)

3 Summary description

Table 5. Truth table

Function									Output
CMD-dir	**DAT0-dir**	**DAT123-dir**	**CMD.h**	**CMD**	**DAT0.h**	**DAT0**	**DAT1.h DAT2.h DAT3.h**	**DAT1 DAT2 DAT3**	
H	X	X	INPUT	OUTPUT	X	X	X	X	B = A
L	X	X	OUTPUT	INPUT	X	X	X	X	A = B
X	H	X	X	X	INPUT	OUTPUT	X	X	B = A
X	L	X	X	X	OUTPUT	INPUT	X	X	A = B
X	X	H	X	X	X	X	INPUT	OUTPUT	B = A
X	X	L	X	X	X	X	OUTPUT	INPUT	A = B

Note: X = Don't care; Z = High impedance

Obsolete Product(s) - Obsolete Product(s)

4 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltage	-0.5 to 4.6	V
V_{CCB}	Supply voltage	-0.5 to 4.6	V
V_I	DC input voltage	-0.5 to 4.6	V
$V_{I/OA}$	DC I/O voltage (output disabled)	-0.5 to 4.6	V
$V_{I/OB}$	DC I/O voltage (output disabled)	-0.5 to 4.6	V
$V_{I/OA}$	DC output voltage	-0.5 to V_{CCA} + 0.5	V
$V_{I/OB}$	DC output voltage	-0.5 to V_{CCB} + 0.5	V
I_{IK}	DC input diode current	-20	mA
I_{OK}	DC output diode current	-50	mA
I_{OA}	DC output current	±50	mA
I_{OB}	DC output current	±50	mA
I_{CCA}	DC V_{CC} or ground current	±100	mA
I_{CCB}	DC V_{CC} or ground current	±100	mA
P_L	Power dissipation	400	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec.)	260	°C

Table 7. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltage	1.4 to V_{CCB}	V
V_{CCB}	Supply voltage	1.4 to 3.6	V
V_I	Input voltage (CMD-dir/DAT0-dir/DAT123-dir)	0 to V_{CCA}	V
$V_{I/OA}$	I/O voltage	0 to V_{CCA}	V
$V_{I/OB}$	I/O voltage	0 to V_{CCB}	V
T_{op}	Operating temperature	-40 to +85	°C
dt/dv	Input rise and fall time (1)	0 to 10	ns/V

1. V_{IN} from 0.8 V to 2.0 V at V_{CC} = 3.0 V

Obsolete Product(s) - Obsolete Product(s)

5 DC and AC parameters

Table 8. DC specification

Symbol	Parameter	Test conditions			Value				Unit
		V_{CCA} (V)	V_{CCB} (V)		T_A = 25 °C		-40 to 85 °C		
					Min.	Max.	Min.	Max.	
V_{IH} (A port)	High level input voltage	1.4-1.95	V_{CCA} to 3.6		0.65V_{CCA}		0.65V_{CCA}		V
		1.95-2.7			1.7		1.7		
		2.7-3.6			2.0		2.0		
V_{IL} (A port)	Low level input voltage	1.4-1.95	V_{CCA} to 3.6			0.35V_{CCA}		0.35V_{CCA}	V
		1.95-2.7				0.7		0.7	
		2.7-3.6				0.8		0.8	
V_{IH} (B port)	High level input voltage	1.4 to V_{CCB}	1.4-1.95		0.65V_{CCB}		0.65V_{CCB}		V
			1.95-2.7		1.7		1.7		
			2.7-3.6		2.0		2.0		
V_{IL} (B port)	Low level input voltage	1.4 to V_{CCB}	1.4-1.95			0.35V_{CCB}		0.35V_{CCB}	V
			1.95-2.7			0.7		0.7	
			2.7-3.6			0.8		0.8	
V_{OH} (A port)	High level output voltage	1.4-3.6	1.4-3.6	I_{OH} = -100µA	V_{CCA}-0.1		V_{CCA}-0.1		V
		1.4	1.4	I_{OH} = -1 mA	1.20		1.20		
		1.65	1.65	I_{OH} = -2 mA	1.40		1.40		
		2.3	2.3	I_{OH} = -4 mA	1.90		1.90		
		3	3	I_{OH} = -8 mA	2.45		2.45		
V_{OL} (A port)	Low level output voltage	1.4-3.6	1.4-3.6	I_{OL} = 100µA		0.10		0.10	V
		1.4	1.4	I_{OL} = 1 mA		0.20		0.20	
		1.65	1.65	I_{OL} = 2 mA		0.25		0.25	
		2.3	2.3	I_{OL} = 4 mA		0.40		0.40	
		3	3	I_{OL} = 8 mA		0.55		0.55	
V_{OH} (B port)	High level output voltage	1.4-3.6	1.4-3.6	I_{OH} = -100µA	V_{CCA}-0.2		V_{CCA}-0.2		V
		1.4	1.4	I_{OH} = -1 mA	1.05		1.05		
		1.65	1.65	I_{OH} = -4 mA	1.20		1.20		
		2.3	2.3	I_{OH} = -6 mA	1.75		1.75		
		3	3	I_{OH} = -8 mA	2.30		2.30		

Obsolete Product(s) - Obsolete Product(s)

Table 8. DC specification (continued)

Symbol	Parameter	Test conditions			Value				Unit
		V_{CCA} (V)	V_{CCB} (V)		T_A = 25 °C		-40 to 85 °C		
					Min.	Max.	Min.	Max.	
V_{OL} (B port)	Low level output voltage	1.4-3.6	1.4-3.6	I_{OL} = 100 µA		0.20		0.20	V
		1.4	1.4	I_{OL} = 1 mA		0.35		0.35	
		1.65	1.65	I_{OL} = 4 mA		0.45		0.45	
		2.3	2.3	I_{OL} = 6 mA		0.55		0.55	
		3	3	I_{OL} = 8 mA		0.70		0.70	
I_{IA}	Input leakage current for A side	1.8	2.9	V_{IA}=V_{CC} or GND DIR=HIGH V_{CD}=V_{WP}=V_{CCA}		±0.5		±5	µA
I_{IB}	Input leakage current for B side	1.8	2.9	$V_{CLK.h}$=V_{CCA} V_{CMD}= V_{CCB} $V_{DAT0,DAT1,DAT2}$=V_{CCB} V_{DAT3}=GND DIR=LOW V_{CD}=V_{WP}=V_{CCA}		±0.5		±5	µA
I_{CCA}	Quiescent supply current for A side	1.65	3.6	V_{IA}=V_{CCA} or GND V_{CD}=V_{WP}=V_{CCA} DIR=HIGH		0.5		5	µA
		1.8	2.5						
		1.8	2.6						
		3.6	3.6						
I_{CCB}	Quiescent supply current for B side	1.65	3.6	$V_{CLK.h}$=V_{CCA} or GND V_{IB}=OPEN DIR=LOW V_{CD}=V_{WP}=V_{CCA}		0.5		5	µA
		1.8	2.5						
		1.8	3.6						
		3.6	3.6						
I_{WP}	WP pin input leakage current	1.8	3.0	V_{IA}=V_{CCA} or GND DIR=HIGH V_{WP}=GND		36			µA
I_{CD}	CD pin input leakage current	1.8	3.0	V_{IA}=V_{CCA} or GND DIR=HIGH V_{CD}=GND		36			µA

Obsolete Product(s) - Obsolete Product(s)

Table 9. AC electrical characteristics (f = 1 MHz, 50% duty cycle, C_L = 30 pF, R_L = 500 Ω)

Symbol		Parameter	Test condition T_A = -40 to 85 °C						Unit
			V_{CCA} = 1.8 ± 0.15V		V_{CCA}=1.8 ± 0.15V		V_{CCA}=2.5 ± 0.2V		
			V_{CCB}=2.5 ± 0.2V		V_{CCB}=2.7 ± 0.3V		V_{CCB}=2.7 ± 0.3V		
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}		Propagation delay time An to Bn	1.0	7.2	1.0	6.6	1.0	6.1	ns
t_{PLH} t_{PHL}		Propagation delay time Bn to An	1.0	8.1	1.0	7.5	1.0	5.0	ns
t_{OSLH} t_{OSHL}		Output to output skew time (1)(2)		0.5		0.5		0.5	ns
t_{CDLH} t_{CDHL}		Clock and data skew time		0.5		0.5		0.5	ns
f_{max}	Clock	From A to B	52		52		52		MHz
		From B to A	52		52		52		
	Data	From A to B	52		52		52		Mbps
		From B to A	52		52		52		

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = | t_{PLHm} = t_{PLHn} |, t_{OSHL} = | t_{PHLm} – t_{PHLn} |)
2. Parameter guaranteed by design.

Table 10. Output slew rate (f = 1 MHz, 50% duty cycle, CL = 15 pF, RL=500 Ω)

Symbol	Parameter	From	To	Test condition T_A = -40 to 85 °C		Unit
				V_{CCA} = 1.8V ± 0.15V V_{CCB} = 3V ± 0.3V		
				Min.	Max.	
t_r	Rise time	10%	90%		3	ns
t_f	Fall time	90%	10%		3	ns

Table 11. Capacitance characteristics

Symbol	Parameter	Test condition			Value					Unit
		V_{CCB} (V)	V_{CCA} (V)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
C_{INB}	Input capacitance	open	open			9				pF
$C_{I/OA}$	Input/output capacitance for A-side	3.3	2.5			17				pF
$C_{I/OB}$	Input/output capacitance for B-side	3.3	2.5			33				pF
C_{PD} (1)	Power dissipation capacitance	3.3	2.5	f = 10 MHz		29				pF
		3.3	1.8			29				

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average current can be obtained by the following equation. I_{CC}(opr) - C_{PD} x V_{CC} x f_{IN} + I_{CC}/16 (per circuit)

Note: V_{IA} = Input I/Os including CLK.h, CMD.h, DAT0.h, DAT1.h, DAT2.h, DAT3.h
V_{IB} = Input I/Os including CMD, DAT0, DAT1, DAT2, DAT3

Obsolete Product(s) - Obsolete Product(s)

6 I/O and test circuit

Figure 3. Input and output equivalent circuit

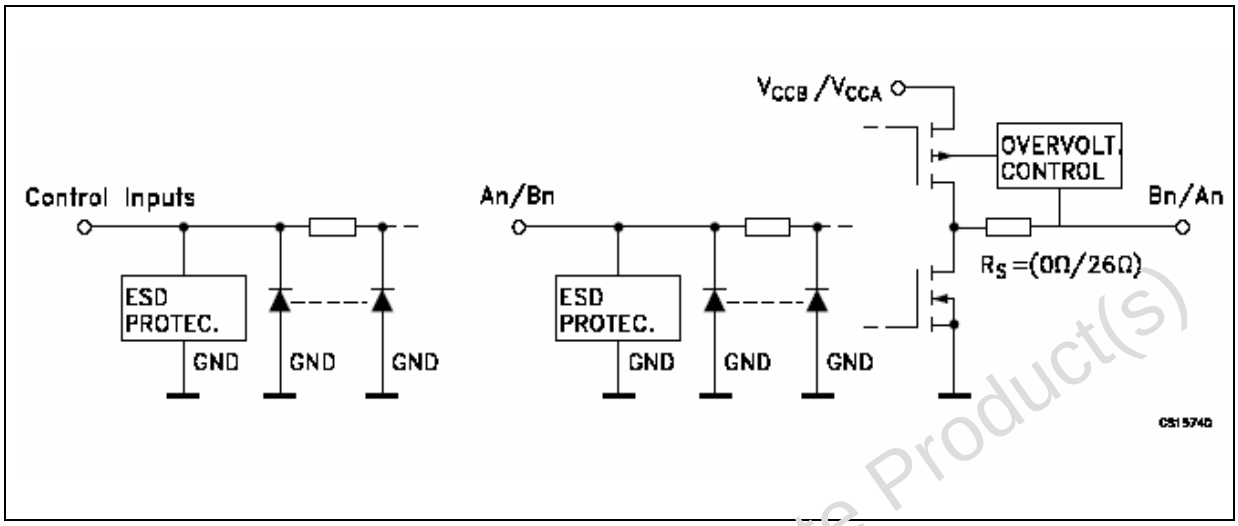
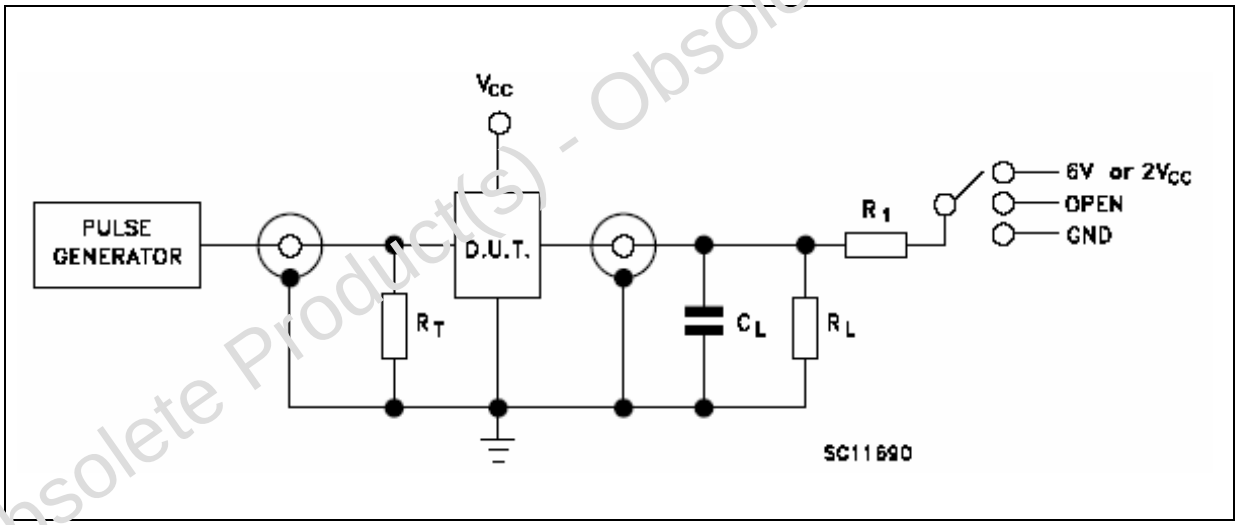


Figure 4. Test circuit



Obsolete Product(s) - Obsolete Product(s)

Table 12. Test values

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ} (V_{CC} = 3.0 to 3.6 V)	6 V
t_{PZL}, t_{PLZ} (V_{CC} = 2.3 to 2.7 V or V_{CC} = 1.6 to 1.95 V)	2 V_{CC}
t_{PZH}, t_{PHZ}	GND

7 Waveforms

Figure 5. Waveform - propagation delay (f = 1 MHz, 50% duty cycle)

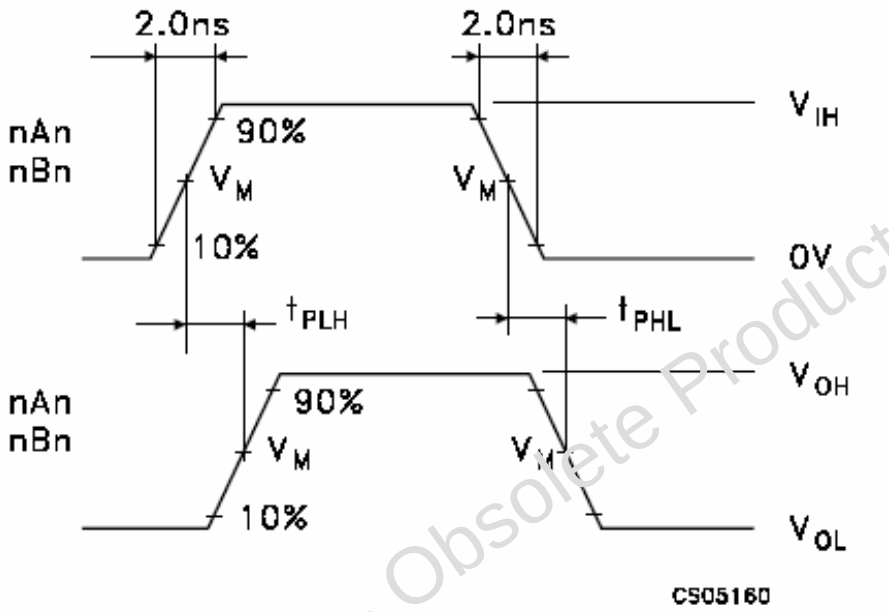


Table 13. Waveform symbol value

Symbol	V_{CC}		
	3.0 to 3.6 V	2.3 to 2.7 V	1.65 to 1.95 V
V_I	V_{CC}	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL}+0.3 V	V_{OL}+0.15 V	V_{OL}+0.15 V
V_Y	V_{OL}-0.3 V	V_{OL}-0.15 V	V_{OL}-0.15 V

Note: C_L = 15 pF for output slew rate measurement
R_L = R1 = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Obsolete Product(s) - Obsolete Product(s)

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 14. µTFBGA25 mechanical data

Dim Ref	Dimension (mm)			Dimension (inch)		
	Min.	Typ.	Max	Min.	Typ.	Max
A	1.0	1.10	1.16	0.039	0.043	0.046
A1			0.25			0.010
A2	0.78		0.86	0.031		0.034
b	0.25	0.30	0.35	0.010	0.012	0.014
D	2.90	3.0	3.10	0.114	0.118	0.122
D1		2.0			0.079	
E	2.90	3.0	3.10	0.114	0.118	0.122
E1		2.0			0.079	
e		0.50			0.020	
SE		0.25			0.010	

Obsolete Product(s) - Obsolete Product(s)

Figure 6. Package dimensions

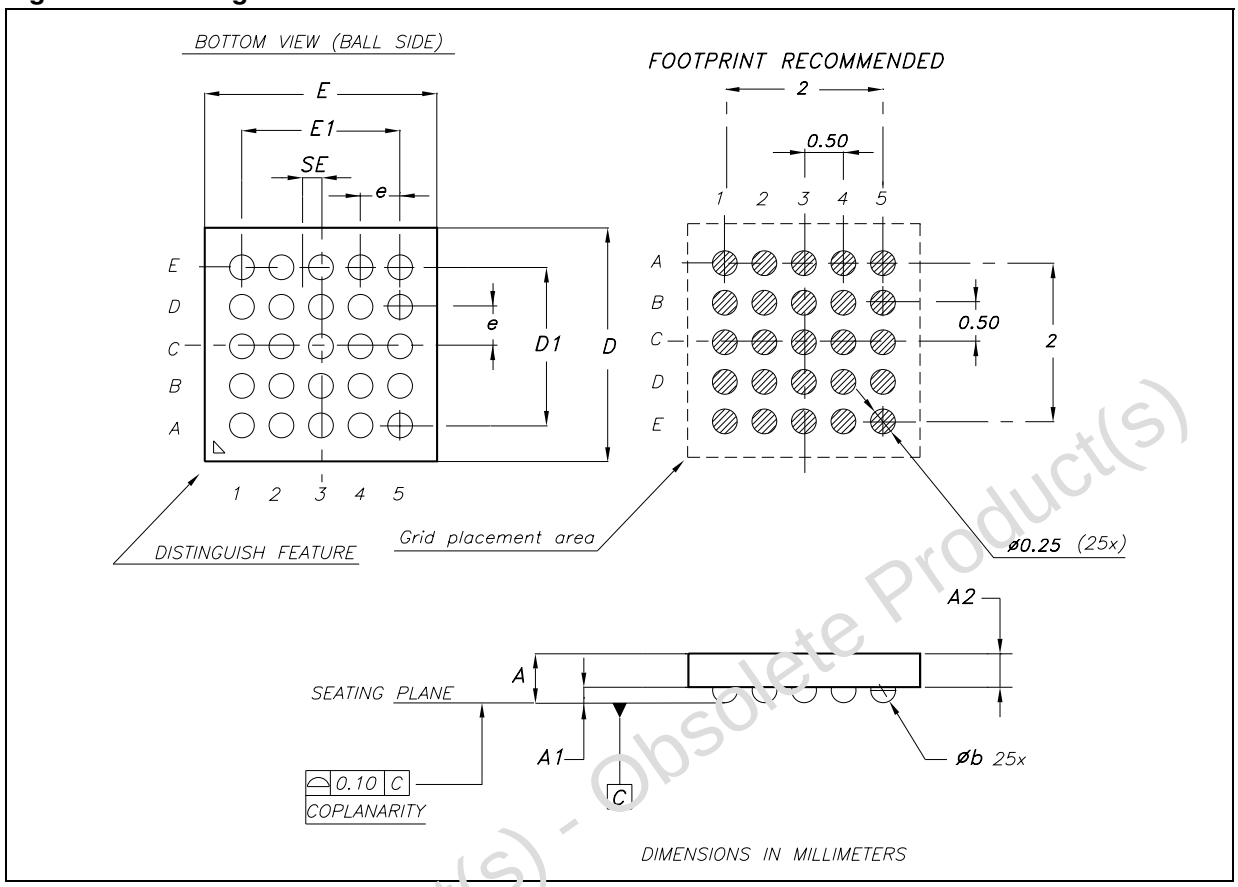


Table 15. µTFBGA25 tape and reel information

Dim Ref	Dimension (mm)			Dimension (inch)		
	Min.	Typ.	Max	Min.	Typ.	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.60			0.063	
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

Obsolete Product(s) - Obsolete Product(s)

Figure 7. Reel dimension

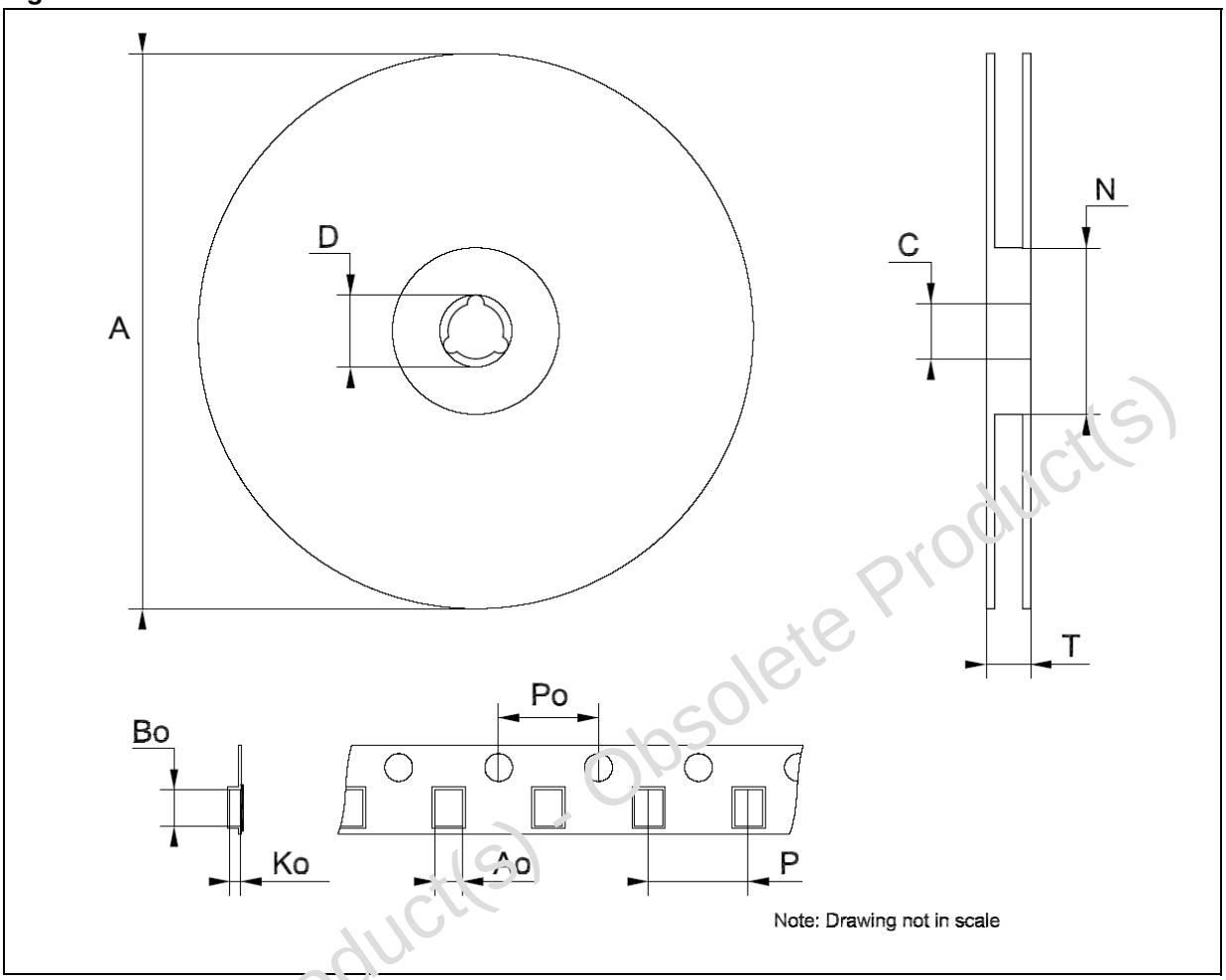


Table 16. TSSOP24 mechanical data

Dim Ref	Dimension (mm)			Dimension (inch)		
	Min.	Typ.	Max	Min.	Typ.	Max
A			1.10			0.043
A1	0.05		0.15	0.002		0.006
A2		0.90			0.035	
b	0.19		0.30	0.007		0.012
C	0.09		0.20	0.004		0.008
D	7.70		790	0.303		31.102
E	4.3		4.50	0.169		0.177
e		0.65			0.026	
H	6.25		6.50	0.246		0.256
L	0.50		0.70	0.020		0.028
K	0º		8º	0º		8º

Obsolete Product(s) - Obsolete Product(s)

Figure 8. Package dimensions

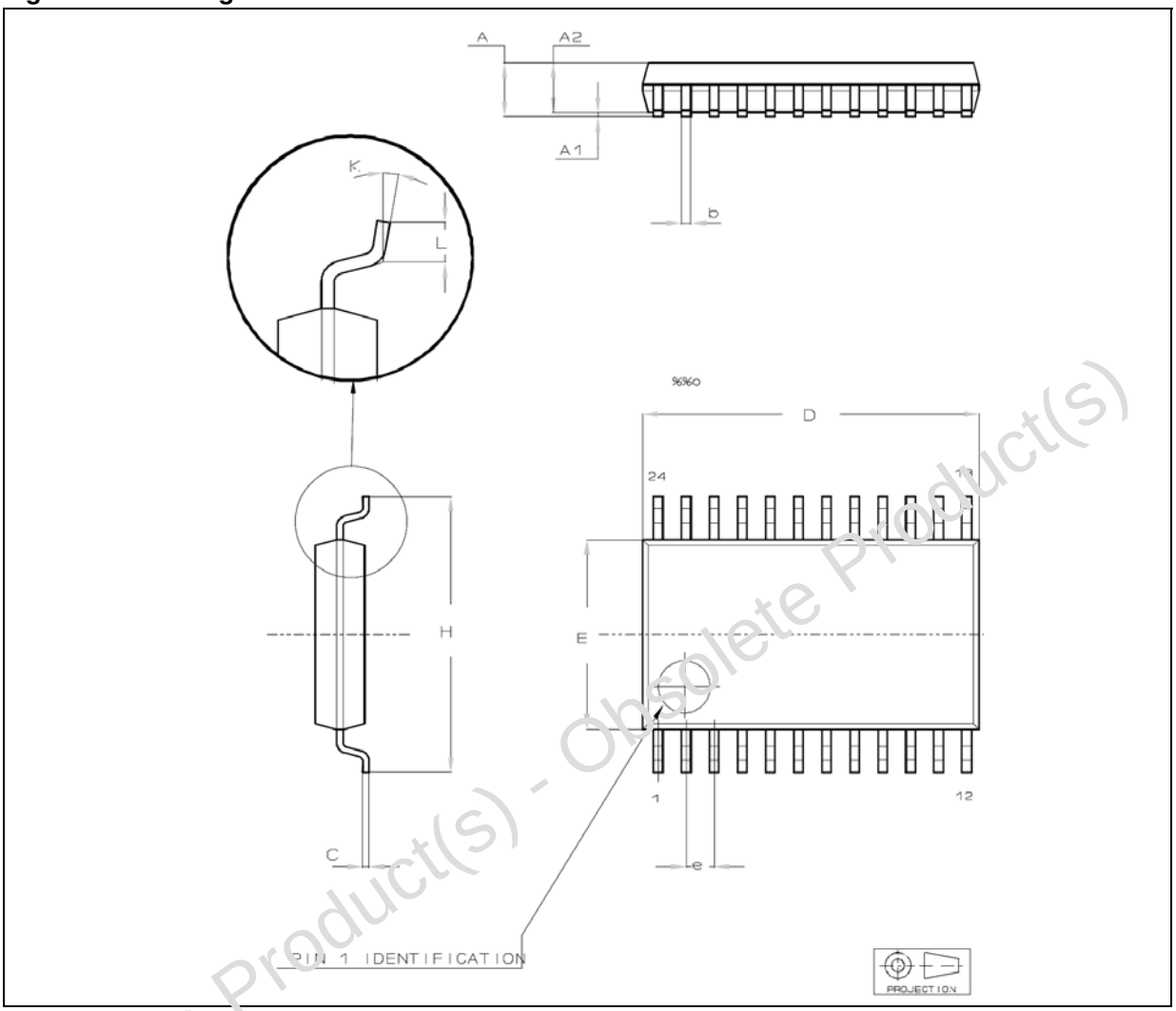
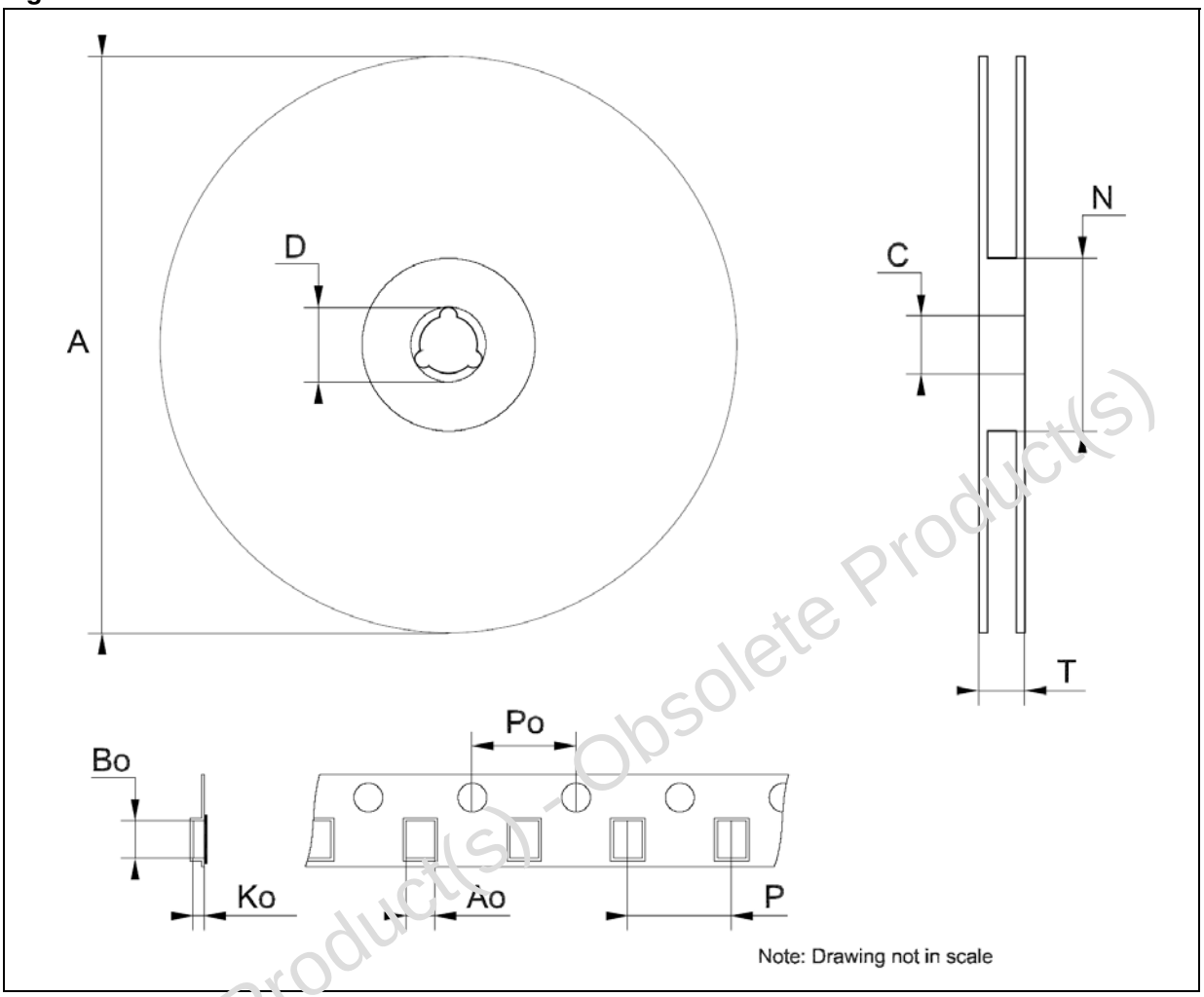


Table 17. TSSOP24 tape and reel information

Dim. Ref	Dimension (mm)			Dimension (inch)		
	Min.	Typ.	Max	Min.	Typ.	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	8.2		8.4	0.323		0.331
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

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Figure 9. Reel dimension



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9 Revision history

Table 18. Document revision history

Date	Revision	Changes
10-Feb-2006	1	First Release
23-Feb-2006	2	New Template
16-Aug-2006	3	Values updated in *Table 8: DC specification on page 8*
04-Aug-2008	4	Changed title of *Table 1* to Device summary, and modified column titles. Changed the C_L value to 15 pF and modified rise and fall t me fro n/to percentages in *Table 10 on page 10*. Modified the C_L value and text in the *Note: on page 12*. Changed title of *Table 18* to Document revision history. Minor text changes throughout the docume nt.

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